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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,071	06/13/2001	Spencer M. Gold	SMQ-042	8019
959	7590	06/30/2005	EXAMINER	
LAHIVE & COCKFIELD, LLP. 28 STATE STREET BOSTON, MA 02109			COLEMAN, ERIC	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/881,071	GOLD ET AL.
	Examiner Eric Coleman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 13 April 2005.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-50 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 1-20 and 29-48 is/are allowed.  
 6) Claim(s) 21-28,49-50 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
     Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
     Paper No(s)/Mail Date. \_\_\_\_\_

5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_

## DETAILED ACTION

### ***Specification***

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The Examiner respectfully asserts that the title is not clearly indicative of the invention. The title does not give enough description as to what differentiates the invention from other systems and indicate what makes it a unique invention. The fact that the free list in the invention is capable of being flushed is not necessarily a new idea. Any free list is capable of being flushed, though in many systems this flushing may have adverse effects. The Examiner asks Applicant to please edit the title to be more descriptive of the invention in the sense of what is new in the art.

### ***Claim Objections***

2. Claims 5-17,19-20,34-45, and 47-48 are objected to because of the following informalities: they are in improper dependent form. MPEP §608.01(n) states that a claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It is also noted that any claim may depend on a previous independent claim. In general applicant's sequence will not be changed.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 21-28,49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeager (patent No. 5,758,112) in view of Rodgers (patent No. 6,889,319).

5. Yeager taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) a structure (figure 1, elements 204, 206,,208 and 210) to track register allocation for a first thread and a second thread of said multithreading microprocessor; [column 8, lines 27-33 show that a register mapping table maps or allocates physical registers to logical registers for integer instructions.];

b) tracking a first set of pointers in said structure assigned to manage said register allocation for an instruction of said first thread of said multithreading microprocessor to prevent a register allocated as a destination operand for said instruction of said thread from being overwritten before said instruction of said first thread retires, [column 12, lines 52-56 show that a free list tracks available integer registers that are unused or free and may be assigned for and instruction destination. Column 13, lines 1-14 show a set of pointers (write pointer, read pointer, and graduation mask). Column 8 lines 1-17 show that a physical register is prevented from being overwritten since it is written to only once before the value is sent back to a logical register and the physical register is free again. Column 14, lines 32-34 show that physical registers are put back in the free list (and marked free) when an instruction graduates or retires. Thus the physical register is not overwritten until the instruction retires]; and

c) tracking a second set of pointers in said structure assigned to

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manage said register allocation for an instruction of said second thread of said multithreading processor to prevent a register allocated as a destination operand for said instruction of said second thread from being overwritten before said instruction of said second thread retires, whereby said first set of pointer and said second set of pointers track independently of each other. [The sections cited above also show the floating-point instructions have renamed registers and a separate free list (figure, element 208) and mapping table (element 204) for the same purpose as integer instructions (not separate structures but separate parts). Figure 1 shows that the mapping and list structures for each are in two separate flows of control and thus two separate threads.

6. Yeager however did not expressly detail (claims 21,23,28,49) that a single structure to track register allocation for a first and second thread. Rodgers taught a single structure (103)(e.g., fig. 3) or (162)(e.g., see fig 6a) or (180)(e.g., see figs. 9 and 10) and col. 11, line 38-col. 14, line 26).

7. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Yeager and Rodgers. Addition of the Rodgers teachings of providing a single structure for tracking multiple threads would have provided increased utilization of shared resources as taught by Rodgers (e.g., see col. 2, lines 14-17). Consequently one of ordinary skill would have been motivated to incorporate the Rodgers teaching of a single structure to track multiple threads to provide greater utilization of shared resources and ultimately to possibly allow for reduction in the size of the system.

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8. In regard to claim 22, Yeager taught a semiconductor device figure 1, microprocessor) having a plurality of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out-of-order execution (column 1, lines 56-59), comprising:

a. a first module (figure, elements (204) 206,208) providing a structure for holding information available physical registers for said microprocessor; [ Column 8, lines 27-33 show that a register mapping table maps or allocates physical registers to logical registers for integer instruction.]

b. a first set of register pointers assigned to a first portion of said structure to track said physical registers assigned as said destination registers for a first thread of said microprocessor, said first set of pointer includes a retire row pointer to identify where a pointer pointing to at least one of said plurality of physical registers assigned as a destination register for an instruction in said first thread that is next to be retired and a read point to identify where a pointer pointing to an available physical register available for assignment as a destination operand for an instruction for said first thread, wherein said microprocessor issues a flush request for said instruction in said first thread, moving said read pointer of said first set of register pointers to said physical register assigned as said destination register for said instruction being flushed in said first thread to restore said physical register to a previous state. [Column 12, lines 52-56 show that a free list tracks available integer registers that are unused or free may be assigned for an instruction destination. Column 13, lines 1-14, show a set of pointers (write pointer, read pointer, and graduation mask). Column 8, lines 1-17 show that a

physical register is prevented from being overwritten since it is written only once before the value is send back to a logical register and the physical register is free again.

Column 14, lines 32-34 show that the physical register is free again. Column 14, lines 32-34) show that the physical registers are put back in the free list (and marked as free when an instruction retires. Thus the physical register is not rewritten until the instruction retires. Column 16, lines 24-26, show that in case of an exception that mappings of register allocation must be restored and this is done by aborting or flushing subsequent instructions (which have not yet committed) and adjusting the read pointer. Column 13, lines 12-14 and column 14, lines 39-43 show that a graduation mask or retire pointer indicated the next graduating or retiring instruction group, where the one selected can be viewed as of a certain row and thus a row pointer is used. The included dictionary definition of "pointer" (third definition) defines a pointer to be a physical or symbolic identifier of a unique target. With this definition, the graduation mask of Yeager, which is shown in column 13, lines 12-13, to identify which instructions graduate or retire, is in fact a retire pointer. The graduation mask identifies a unit target, the instructions to graduate or retire.

9. Yeager disclosed a graduation mask for identifying which instruction graduated (retired). Yeager did not expressly detail (claim 22) use of a retirement pointer. Rodgers however taught a retirement pointer (elements 182, and 183) (e.g., see retirement pointers 182 and 183, in fig. 10 and col. 12, lines 2-44).

10. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Yeager and Rodgers. Addition of the Rodgers teachings of providing a

single structure for tracking multiple threads would have provided increase utilization of shared resources as taught by Rodgers (e.g., see col. 2, lines 14-17). Consequently one of ordinary skill would have been motivated to incorporate the Rodgers teaching of a single structure to track multiple threads to provide greater utilization of shared resources and ultimately to possibly allow for reduction in the size of the system.

11. In regard to claim 23, Yeager discloses the semiconductor device of claim 22, further comprising a second set of register pointers to a second portion of said structure to track said physical registers assigned as said destination registers for a second thread of said microprocessor and when said microprocessor issues a flush request for an instruction in said second thread, moving a read pointer of said second set of register pointers to said physical register assigned as said destination register for said instruction being flushed in said second thread to restore said physical register to a previous state [The sections cited above also show that floating point-instructions have renamed registers an a separate free list (figure 1, element 208) and mapping table (element 204) for the same purpose as integer instructions. Figure 1 shows that the mapping and list structures for each are in two separate flows of control and thus two separate threads.]

12. In regard to claim 24, Yeager discloses the semiconductor of claim 22, wherein said structure comprises a free physical register list for said identification of said available physical requests for said microprocessor (as shown above).

13. In regard to claim 25, Yeager discloses a semiconductor of claim 23, wherein first set of register pointers move independently of said second set of register pointers

wherein said first set of register pointers identify said physical registers assigned to instructions in said first thread of said microprocessor that have not been committed and said second set of register pointers identify said physical registers assigned to instructions in said second thread of said microprocessor that have not been committed. [ As shown above two thread are independent since they have two flows of control. The set of pointers of each thread comprise a read pointer (column 13, lines 1-6). This pointer identifies registers of instructions for allocation (column 14, lines 56-59) that have not yet been committed, since the committing does not occur until the write pointer identifies a register for writing.]

14. In regard to claim 26, Yeager discloses a semiconductor of claim 22, wherein said first set of register pointers further comprises, a write row pointer, wherein said write row pointer identifies where a pointer pointing to said physical register of an instruction in said first thread should be written when said instruction commits.[Column 13, lines 14-16 show that a write row pointer is used. Column 14, lines 20-24 show that this is the place to next write, which happens on a commit when the result is ready.]

15. In regard to claim 27, Yeager discloses the semiconductor device of claim 23, wherein said second set of register pointers further comprises a write row pointer and a retire row pointer, wherein said write row pointer identifies where a pointer pointing to said physical register of an instruction in said second thread that is committed should be written, and said retire row pointer identifies where a pointer pointing to said physical register of an instruction in said second thread that is next to be retired.

[Column 13, lines 14-16 show that a write pointer is used. Column 14, lines 20-24 show that this is the place to next write, which happens on a commit when the result is ready. Column 13, lines 12-14 and column 14, lines 39-43 show that a graduation mask or retire pointer indicate the next graduating or retiring instruction from a group, where the one selected can be viewed as of a certain row and thus a row pointer is used. As shown above the renaming works similar for both threads.]

16. In regard to claim 28, Yeager discloses a semiconductor device having a plurality of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out-of order execution comprising:

- a. a first module (figure 1, elements 204, 206,,208 and 210) providing a structure for holding information identifying available physical registers for said microprocessor ;[column 8, lines 27-33 show that a register mapping table maps or allocates physical registers to logical registers for integer instructions.];
- b. a first set of register pointers assigned to a first portion of said structure to track said physical registers assigned to said destination registers for a first thread of said microprocessor and when said microprocessor issues a flush request for an instruction in said first thread, moving a read pointer of said first set of register pointers to said physical register assigned as said destination register for said instruction being flush in said thread to restore said physical register to a previous state.[Column 12, lines 52-56 show that a free list tracks available integer registers that are unused or free may be assigned for an instruction destination. Column 13, lines 1-14, show a set of pointers (write pointer, read pointer, and graduation mask). Column 8, lines 1-17 show

that a physical register is prevented from being overwritten since it is written only once before the value is send back to a logical register and the physical register is free again. Column 14, lines 32-34 show that the physical register is free again. Column 14, lines 32-34) show that the physical registers are put back in the free list (and marked as free when an instruction retires. Thus the physical register is not rewritten until the instruction retires. Column 16, lines 24-42, show that in case of an exception the mappings of register allocation must be restored and this is done by aborting or flushing subsequent instructions (which have not yet committed) and adjusting the read pointer.]

c. and a second set of register pointers assigned to a second portion of said structure to track said physical registers assigned as said destination registers for a second thread of said microprocessor and when said microprocessor issues a flush request for an instruction in said second thread, moving a read pointer of said second set of register pointers to said physical register assigned as said destination register for said instruction being flushed in said second thread to restore said physical register to a previous state. [The sections cited above also show that floating-point instructions have renamed registers and a separate free list (figure, element 208) and mapping table (element 204) for the same purpose as integer instructions (separate meaning different parts of the same structure). Figure 1 show that the mapping and list structures for each are in two separate flows of control and thus two separate threads.

17. In regard to claim 49, Yeager discloses a computer readable medium (figure 1, element 102) holding computer executable instructions for performing a method in a

multithreading microprocessor performing speculative instruction execution (figure 1, and column 2, lines 40-42), said method comprising the steps of:

- a. providing a structure (figure 1, elements 204, 206,,208 and 210) to track register allocation for a first thread and a second thread of said multithreading microprocessor; [column 8, lines 27-33 show that a register mapping table maps or allocates physical registers to logical registers for integer instructions.];
- b. tracking a first set of pointers in said structure assigned to manage said register allocation for an instruction of said first thread of said multithreading processor to prevent a register allocated as a destination operand for said instruction of said thread from being overwritten before said instruction of said first thread retires, [column 12, lines 52-56 show that a free list tracks available integer registers that are unused or free and may be assigned for and instruction destination. Column 13, lines 1-14 show a set of pointers (write pointer, read pointer, and graduation mask). Column 8 lines 1-17 show that a physical register is prevented from being over written since it is written to only once before the value is sent back to a logical register and the physical register is free again. Column 14, lines 32-34 show that physical registers are put back in the free list (and marked free) when an instruction graduates or retires. Thus the physical register is not overwritten until the instruction retires];
- c. tracking a second set of pointers in said structure assigned to manage said register allocation for an instruction of said second thread of said multithreading processor to prevent a register allocated as a destination operand for said instruction of said second thread from being overwritten before said instruction of said second

thread retires, whereby said first set of pointer and said second set of pointers track independently of each other. [The sections cited above also show the floating-point instructions have renamed registers and a separate free list (figure, element 208) and mapping table (element 204) for the same purpose as integer instructions (not separate structures but separate parts). Figure 1 shows that the mapping and list structures for each are in two separate flows of control and thus two separate threads.]

18. As to claim 50, Rodgers discloses wherein the single structure includes at least one protected register region identifying physical pointers allocated to instructions having logical destination register decoded and issued but not yet retired (e.g., see fig.5,6a,9 and col. 11, line 38-col. 12, line 64 and col. 20, lines 1-53).

***Allowable Subject Matter***

19. Claims 1-20 and 29-48 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



ERIC COLEMAN  
PRIMARY EXAMINER